

Steve Morris

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Objective: Lead engineer/supervisor using my strengths either in embedded software engineer design verification, preferably both.

Experience:

2007-2008

Director Verification Products; Gaterocket Inc. Bedford, MA

The product accelerated FPGA RTL simulation by loading code into the actual target FPGA and then transparently connecting it to the verification simulation testbench.

- Implemented complete system simulation model of multi board, multi chip product including a Linux pseudo PCI driver which talked to hardware simulation allowing the actual application binaries to run against the hardware simulation model before arrival of hardware.
- Enhanced RTL communication code which implemented the core interface between the various boards and eventually the Testbench running on the Linux PC.
- Implemented an automated test regression system
- Coded for small CPU used to drive various sensors
- Implemented interface code in PLI, VHPI, FLI, and SystemC for Cadence, Synopsis and Modeltech Verilog and VHDL simulators.

2002-2007

Design Verification Technical lead; Teradyne Inc. North Reading, MA;

- Lead for system simulation group which released 3 ASICS with only one minor metal layer respin.
- Principal SystemC and C++ architect of a testbench environment eventually used by many verification projects within Teradyne..
- General perl toolsmith.
- Verification project lead for an outsourcing project which included 6 US engineers and 18 engineers in India. This was a first for the company so it required substantial invention of outsourcing methodology to overcome the many potential pitfalls of such a relationship. The project was a success.

2000-2002

Design Verification Technical lead; Cereva Networks Inc; Marlborough, MA

- Coordinated efforts of a 5 person Verification group responsible for verification of 9 Xilinx VirtexE FPGAs and 3 CPLDs for the Cereva 5000 Fibre Channel based Storage system.
- Implemented testbenches, wrote transactors (in Verilog) and tests in C++ for most of the FPGAs.
- Created a substantial number of tools in perl including front ending source control and running automated regressions.
- The testbench environment was MintSim, a C++ based tool implemented with a PLI interface.

1998-2000

Fujitsu Nexion; Acton, MA

ASIC manager

- Managed the development of small ASIC group with responsibility for design, DV, board design and backend. Assumed project responsibility when lead designers quit.

Lead Design Verification engineer

- Supervised 3 person DV team
- 2 ASICs on a channelized/unchannelized T3/E3 Frame Relay to ATM card for the Nexen 8000.
- The testbench environment was VDB, a Nexion proprietary tool based in C++ and Tcl.
- Verified FRF-5, FRF-8, rate policing, HDLC.

1988-1998

Xionics Document Technologies; Burlington, MA

1995-1998 Lead ASIC Design Verification Engineer

- Verified XipChip a 500k gate ASIC with PPC 401 core plus many image processing and device interface coprocessors to implement scanner/printer/fax application. Implemented testbenches and wrote tests in Verilog and PowerPC assembler.
- Verified Xionics first ASIC. Verification methodology was to test synthesized Verilog in realtime in 9 FPGA's. Verification software was essentially the board diagnostics software plus the application software. By using FPGA's the application development went in parallel to the timing, backend and fabrication steps of ASIC development.

1988-1995 Director of Porting

- Hands on manager of porting the core Postscript and PCL-5 applications from UNIX to Printer Raster Image Processors in over 14 printers. Managed development of reference platform RIP controller board and then successive respins target towards several customers printer controller needs.
- Ported Appletalk/LocalTalk PAP interface.
- Delivered 14 customer ports including Xerox, Calcomp and Seiko

- Installed and implemented the software tool chain for 5 microprocessors
- BSP development.
- Supported lab bringup of many printer controller boards.

1987–1988

Software Director; Analytix; Cambridge, MA

- Ran the 3 person software group in this small startup. Software was C++ based for the 68000 and assembler for the 68hc11 and included robot control (stepper motors and sensors) and simple chemical analysis. This startup folded while I was there which explains my short tenure.
- Implemented stepper motor arm controller and navigation system
- Implemented 16 bit dual slope A/D in software using 8 bit A/D for zero detect for cost reduction.

1980–1987

Lead Software engineer/software manager; Digilab Instruments; Cambridge, MA

- Wrote software for Digilab FTS series FT-IR infrared spectrometers.
- As embedded control programmer debugged boards, ported UNIX and other OS's, developed array processor software for FFT, dot product spectral search and advanced statistics.
- Ported UNIX clone (Idris) to 68000
- Implemented real-time interface to high speed optical bench.
- Developed optical bench control software.
- Designed and implemented multitasking kernel for the 68000.

1977-1980

Systems Analyst; Medical records HCHP; Boston

- As a programmer I supported the COSTAR on line interactive medical record system. The system was written in a dialect of MUMPS.

Languages:

Verilog, VHDL, Postscript, C, C++, Perl, Tcl/Tk, Fortran, 68000, 29k, PowerPC, 68hc11 and 80960 assembler, MUMPS, SQL, HTML, Javascript

Operating systems:

Unix, Windows, VxWorks, pSOS (Note: I have written a preemptive multitasking kernel for the 68000.)

Education:

Physics, University of Massachusetts Boston, MA.

Interests:

Canoeing, hiking, bicycling, robots, coaching soccer, Barbershop quartet singing.